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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,733	10/25/2000	Curtis Priem	18659-15C1	8456

23419 7590 07/30/2004

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EXAMINER	
TUNG, KEE M	

ART UNIT	PAPER NUMBER
2676	19

DATE MAILED: 07/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,733	PRIEM ET AL.	
	Examiner	Art Unit	
	Kee M Tung	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The amendment filed 5/12/04 has been considered in preparing this Office action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 25-29 and 37-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morgan et al (5,821,940 hereinafter "Morgan") in view of Rentschler et al (5,812,950 hereinafter "Rentschler ").

Morgan teaches a graphics system (Fig. 5) comprising a CPU (12) having an associated system memory (not shown, but is inherent by any computer, furthermore, Morgan teaches display list memory is portion of the system memory, col. 3, lines 51-54), said CPU adapted to issue commands for rendering polygons of a graphical image; a graphics module (combination of display list controller 16, transformation processor 18, cache storage means 22 and backend processor 24) coupled to said CPU and said associated system memory by a system bus (the bi-directional bus coupled between display list memory and display list controller, see figure 2), said graphics module comprising a cache (28) for storing vertex data; a cache controller (26) configured to receive a command to render a polygon from said CPU, said cache controller (26) checking said cache (28) for previously cached vertex data for vertices of said polygon; and said graphics module configured to utilize said vertex data to render pixel data for

said polygon. It is noted that in the specification, Morgan called bus 31 as a system bus. It would have been obvious to one of ordinary skill in the art at the time the present invention was made that the bus cannot be the computer's system bus. It is more like an internal bus in the graphics pipelined/subsystem connected between front-end processor (such as, transformation processor 18) and the backend processor 24. Furthermore, Rentschler teaches that there is an internal bus connected between the front-end and backend processors and a host/system bus coupled between host and the front-end processor 10. Therefore, it would have been obvious to one of ordinary skill in the art at the time the present invention was made that the system bus 31 of Morgan can not be the claimed system bus as proved or support by Rentschler. Therefore, at least claim 25 would have been obvious by Morgan.

As per claim 26, Morgan fails to explicitly teach a state machine for directing said cache controller to update said cache. It is noted that a state machine is considered an old and well know feature for the CPU to include. Therefore, claim 26 would have been obvious.

Method claim 37 is similar in scope to system claim 25, and additionally requires index values of cache for vertex data of said vertices of said polygon (col. 3, lines 35-43). Therefore, at least claims 27 and 37 would have been obvious.

Method claim 41 is similar in scope to system claim 25 and method claim 37, and additionally requires performing a memory transfer operation to transfer required vertex data from system memory (from display list memory 14, col. 3, lines 20-43) to cache. Morgan further teaches performing a memory transfer operation to transfer required

vertex data from video memory (14) to cache memory (28). Therefore, at least claims 28-29 and 38-44 would have been obvious.

3. Claims 30-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morgan (5,821,940) in view of Rentschler et al (5,821,950) and Holt et al (5,760,792 hereinafter "Holt").

The teachings of Morgan and Rentschler are given in previous paragraph of this Office action. System claim 30 is similar in scope to system claim 25 and method claims 37 and 41, and additionally requires a DMA engine for transferring vertex data from transfer memory (display list memory 14) to cache (26). Holt teaches a graphics processor board (Fig. 2) comprising a DMA (211) for transferring vertex data from main memory to the graphics FIFO (col. 2, lines 56-61). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Holt into the system of Morgan and Rentschler in order to transfer vertex data from main memory to the graphics cache in high speed, such as, capable of burst transfer as taught by Holt (col. 2, lines 56-61). Therefore, at least claims 30-33 and 36 would have been obvious.

4. Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morgan (5,821,940) in view of Rentschler et al (5,821,950) and Holt et al (5,760,792 hereinafter "Holt") as applied to claim 30 above, and further in view of Porterfield (6,069,638).

The teachings of Morgan, Rentschler and Holt are given in previous paragraph of this Office action. However, the combined system fails to explicitly teach said CPU is

coupled to said system bus by a graphics bridge and said system memory is connected to said graphics bridge. These are what Porterfield teaches (Fig. 3). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Porterfield into the system of Morgan, Rentschler and Holt as claimed in order to add design flexibility to the system. Therefore, at least claims 34 and 35 would have been obvious.

Response to Arguments

5. Applicant's arguments with respect to claims 25-44 have been considered but are moot in view of the new ground(s) of rejection.

Basically, applicant argues that the bus 31 of Morgan is a system bus which has been discussed in the detailed rejection with respect to claim 25 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M Tung whose telephone number is 703-305-9660. The examiner can normally be reached on Tuesday - Friday from 5:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kee M Tung
Primary Examiner
Art Unit 2676